Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L6	8236	(resist or photoresist or mask or photomask) and (insulator or insulative or insulating or dielectric) and (etching with substrate)	USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/02/24 14:18
L7	4613	(resist or photoresist) and (insulator or insulative or insulating or dielectric) and (etching with substrate)	USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/02/24 14:19
L8	1947	(resist or photoresist) and (insulator or insulative or insulating or dielectric) and (etching near5 substrate)	USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/02/24 13:57
L9	48	8 and (trench near isolation)	USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/02/24 14:19
L10	45589	(resist or photoresist or mask or photomask) and (insulator or insulative or insulating or dielectric) and (etching with substrate)	US-PGPUB; USPAT	OR	ON	2005/02/24 14:18
L11	36664	(resist or photoresist) and (insulator or insulative or insulating or dielectric) and (etching with substrate)	US-PGPUB; USPAT	OR	ON	2005/02/24 14:19
L12	22887	(resist or photoresist) and (insulator or insulative or insulating or dielectric) and (etching near5 substrate)	US-PGPUB; USPAT	OR	ON	2005/02/24 14:19
L13	17124	(resist or photoresist) and (insulator or insulative or insulating or dielectric) and (etching near3 substrate)	US-PGPUB; USPAT	OR	ON	2005/02/24 14:19
L15	3024	13 and (trench near isolation)	US-PGPUB; USPAT	OR	ON	2005/02/24 14:20
L16	233	15 and (ARC or antireflective or anitireflection)	US-PGPUB; USPAT	OR	ON	2005/02/24 14:21
L17	199	16 and @ad<"20021030"	US-PGPUB; USPAT	OR	ON	2005/02/24 14:21

	Type	Hits	Search Text	DBs
155	BRS	177	S165 and ((GaN or(gallium adj nitride)) with epitaxial$2)	US-PGPUB; USPAT
156	BRS	9	S167 and 2ad<"22020823"	US-PGPUB; USPAT
157	BRS	9	((pile adj up) with density with dislocation) and germanium	US-PGPUB; USPAT
158	BRS	1	((pile adj up) with density with dislocation) and germanium	USOCR; EPO; JPO; DERWENT; IBM_TDB
159	BRS	4664	438/455,458,795,107,119,22,25,51.ccls.	US-PGPUB; USPAT
160	BRS	3775	S170 and @ad<"20021217"	US-PGPUB; USPAT
161	BRS	45589	(resist or photoresist or mask or photomask) and (insulator or insulative or insulating or dielectric) and (etching with substrate)	US-PGPUB; USPAT
162	BRS	30727	S172 and (substrate with (opening or hole or recess or trench or via or aperture))	US-PGPUB; USPAT
163	BRS	24847	S173 and @ad<"20021030"	US-PGPUB; USPAT
164	BRS	1948	S174 and (ARC or antireflective or antireflection)	US-PGPUB; USPAT
165	BRS	1531	S175 and (substrate near5 (opening or hole or recess or trench or via or aperture))	US-PGPUB; USPAT
166	BRS	1298	S175 and (substrate near3 (opening or hole or recess or trench or via or aperture))	US-PGPUB; USPAT

	Time Stamp	Comments	Error Definition	Errors	Ref #
155	2005/02/17 17:10				S166
156	2005/02/23 15:11				S168
157	2005/02/23 17:49				S167
158	2005/02/23 15:16				S169
159	2005/02/23 17:49				S170
160	2005/02/23 17:50				S171
161	2005/02/24 10:16				S172
162	2005/02/24 10:20				S173
163	2005/02/24 08:51				S174
164	2005/02/24 08:51				S175
165	2005/02/24 08:52				S176
166	2005/02/24 08:52				S177

DOCUMENT-IDENTIFIER: US 20020024111 A1

TITLE: Shallow **trench isolation** type semiconductor device and method of forming the same

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Abstract Paragraph - ABTX (1):
A shallow **trench isolation** type semiconductor device is described, which includes a trench having a flexure in a bottom thereof. The flexure has a step difference of about 100 .ANG. or more, and is preferably made at a middle area. Conventionally, a gate **insulating** layer includes a thin area of about 100 .ANG. or less and a thick area of about 200 .ANG. or more. On the basis of a bottom of a trench peripheral region, a middle part of the flexure may be concave or convex. Particularly, the foregoing device can effectively be applied to a self-aligned flash memory in which a width of a trench between one active region and another is about 3 micrometers or less.

Title - TTL (1):
Shallow **trench isolation** type semiconductor device and method of forming the same

Summary of Invention Paragraph - BSTX (4):
[0003] The present invention generally relates to a shallow **trench isolation** type semiconductor device and a method of forming the same. More specifically, the present invention is directed to a shallow **trench isolation** type semiconductor device in which **insulating** layers differ in thickness according to regions, and a method of forming the same.

Summary of Invention Paragraph - BSTX (6):

[0005] A common problem encountered in device isolation in a high-density semiconductor device is a bird's beak effect, which occurs due to a lateral growth of thermal silicon dioxide in the form of a bird's beak under a SiN.sub.4 protective layer. The bird's beak is undesirable since it takes up needed area and has electrical field effects that permit current leakage. A shallow **trench isolation** (STI) technique for device isolation has been widely used and avoids the problem of the bird's beak effect. However, to achieve superior device isolation results, the depth and width of a trench must be increased. Since it is desirable to have semiconductor devices having small footprints for higher integration, the depth must be increased while the width for insulation must be decreased. In a less than ideal scenario, a deep trench cannot be formed due to the decrease in the width.

Summary of Invention Paragraph - BSTX (7):

[0006] When a high voltage is applied, the component at which a high voltage is applied must have a structure that is able to withstand the high voltage. Typically, a gate **insulating** layer formed at the part where the high voltage is applied is made thicker than the gate **insulating** layer formed at others.

Summary of Invention Paragraph - BSTX (8):

[0007] FIG. 1 is an exemplary cross-sectional view showing the difference in thickness of a gate **insulating** layer at a low voltage part of cell and peripheral regions compared to a gate **insulating** layer at a high voltage part of the peripheral region. FIG. 1 also shows an exemplary formation of a self-aligned trench in each region of a flash memory device in which the gate **insulating** layers differ in thickness. At the peripheral region where the gate **insulating** layer 13 is thickly formed, a trench 17 for device isolation is shallowly formed, which increases the probability that insulation for device isolation will not be sufficient.

Summary of Invention Paragraph - BSTX (9):

[0008] FIG. 1 includes gate **insulating** layers 11 and 13 which differ in thickness according to each region of a substrate 10. Conventionally, the thickness of the gate **insulating** layer 11 formed at a low voltage part of cell and peripheral regions is about 70 .ANG. to about 80 .ANG. and the thickness of the gate **insulating** layer 13 formed at a high voltage part of the peripheral region is about 250 .ANG. to about 350 .ANG.. A polysilicon layer 15 for forming a part of a self-aligned floating gate is stacked on the gate **insulating** layers 11 and 13. Based upon the STI technique, device isolation is then carried out. In other words, an etch-stop layer made of silicon nitride is deposited. Preferably, a high temperature oxide (HTO) layer is then deposited for patterning the etch-stop layer, and an anti-reflection coating (**ARC**) layer is additionally deposited.

Summary of Invention Paragraph - BSTX (10):

[0009] Through **photoresist** coating, exposure using a device isolation mask pattern, and development, a trench pattern for device isolation is formed. Subsequently, upper layers are sequentially etched to be removed. A patterned upper layer can serve as an etching mask to a lower layer. Generally, the etch-stop layer is patterned and the **photoresist** pattern is removed by ashing and stripping techniques. The polysilicon layer 15, the gate **insulating** layers 11 and 13, and the substrate silicon layer 10 are etched to form a trench. In the etching process to form the trench, separately etching the gate **insulating** layer and the substrate causes problems due to shifting of the etching apparatus. Thus, the process is carried out in one etching apparatus (i.e., "in-situ"). It takes a great deal of time to etch a gate **insulating** layer at a part where the gate **insulating** layer is thickly formed. With a conventional silicon oxide layer and silicon etchant for forming a trench, a depth difference (A) of about 180 .ANG. to about 500 .ANG. is observed in a substrate trench where the gate **insulating** layer is thickly formed. Naturally, the depth difference (A) varies according to the type of etchant used.

Summary of Invention Paragraph - BSTX (11):

[0010] Preferably, after thinly stacking a sidewall oxide layer and a silicon nitride liner, the trench is filled with a CVD oxide layer. To complete the **trench isolation** layer 17, a chemical mechanical planarization (CMP) process for removing the stacked CVD oxide layer on a region except the trench, a wet etching process to remove an etch-stop layer made of silicon nitride, and a cleaning process are then performed. However, where the gate insulation layer is thickly formed, a thickness of the isolation layer 17 has a depth difference (A) as great as a depth of the trench. This is disadvantageous, since if the isolation layer 17 becomes thin at a transistor peripheral region to which a high voltage is applied, device isolation can be incomplete.

Summary of Invention Paragraph - BSTX (12):

[0011] Therefore, a need exists for a shallow **trench isolation** type semiconductor device and a method of forming the same, which can complement a **trench isolation** layer whose thickness in a silicon substrate is not sufficient. A need also exists for a shallow **trench isolation** type semiconductor device and a method of forming the same which can complement incomplete device isolation caused by a **trench isolation** layer whose thickness in a silicon substrate is not sufficient in certain regions due to a thicker gate **insulating** layer. Additionally, a need exists for a shallow **trench isolation** type semiconductor device and a method of forming the same which can complement a device isolation layer whose thickness is not sufficient without causing an aligning problem.

Summary of Invention Paragraph - BSTX (14):

[0012] According to an aspect of the present invention, a shallow **trench isolation** type semiconductor device is provided wherein a flexure with a step difference is made at a bottom of a trench. Specifically, a shallow **trench**

isolation type semiconductor device is provided including at least two regions where gate **insulating** layers differ in thickness; and a silicon substrate with at least one flexure trench having a step difference.

Summary of Invention Paragraph - BSTX (15):

[0013] At least in a partial region of the semiconductor device, a gate **insulating** layer is deposited at a thickness of about 200 .ANG. or more. Conventionally, the gate **insulating** layer has a thin region of about 100 .ANG. or less and a thick region of about 200 .ANG. or more. If a step difference of the gate **insulating** layer is about 100 .ANG., the step difference of about 100 .ANG. will remain in an etching process without an etching selectivity with respect to a silicon oxide layer and a silicon layer. The step difference can be expanded to, for example, about 500 .ANG..

Summary of Invention Paragraph - BSTX (17):

[0015] A typical example of an aspect of the present invention can be shown in a flash memory that has a thick gate oxide layer of about 300 .ANG. or more in a peripheral region, and a thin gate oxide layer of about 80 .ANG. or less in a low voltage part of cell and peripheral regions. Particularly, the typical example is shown in a self-aligned flash memory wherein a polysilicon layer to form a part of a floating gate and a trench etching mask are sequentially deposited on a gate **insulating** layer. The present invention is particularly effective in cases where a width of a trench between one active region and another is 3 micrometers or less at a region having a thick gate oxide layer.

Summary of Invention Paragraph - BSTX (19):

[0017] Specifically, a method of forming a shallow **trench isolation** type semiconductor device according to an aspect of the present invention comprises the steps of: forming a gate oxide layer, so that a flexure is different from adjacent parts in thickness, the flexure being a part of a trench area on a

substrate; forming an etching mask pattern to expose the gate oxide layer in the trench area; and anisotropically and sequentially etching the gate oxide layer and a silicon substrate to form a trench, the gate oxide layer being located on the **substrate where the etching** mask pattern is formed.

Summary of Invention Paragraph - BSTX (20):

[0018] The step of anisotropically etching the gate oxide layer and the silicon **substrate comprises two steps: etching** the gate oxide layer to expose the silicon substrate on the basis of a thin or thick gate oxide area, and **etching the silicon substrate**. In at least one of the two steps, an etchant having a low etching selectivity is used. To completely remove the gate oxide layer at a thick gate oxide area, the silicon substrate is etched in a thin gate oxide area as much as a predetermined thickness according to a kind of etchant. Alternatively, one etchant is used in the two steps.

Brief Description of Drawings Paragraph - DRTX (2):

[0020] FIG. 1 is an exemplary cross-sectional view showing the difference in thickness of a gate **insulating** layer at a low voltage part of cell and peripheral regions compared to a gate **insulating** layer at a high voltage part of the peripheral region.

Brief Description of Drawings Paragraph - DRTX (3):

[0021] FIG. 2 is an exemplary cross-sectional view showing a step of performing self-aligned trench device isolation at a low voltage part in cell and peripheral regions and a high voltage part of the peripheral region during the formation of a NAND-type flash memory according to an aspect of the present invention, wherein gate **insulating** layers that differ in thickness are formed.

Brief Description of Drawings Paragraph - DRTX

(4):

[0022] FIG. 3 is an exemplary cross-sectional view showing a step of performing self-aligned trench device isolation at a low voltage part in cell and peripheral regions and a high voltage part of the peripheral region during the formation of a NAND-type flash memory according to an aspect of the present invention, wherein the gate **insulating** layers are etched.

Brief Description of Drawings Paragraph - DRTX

(5):

[0023] FIG. 4 is an exemplary cross-sectional view showing a step of performing self-aligned trench device isolation at a low voltage part in cell and peripheral regions and a high voltage part of the peripheral region during the formation of a NAND-type flash memory according to an aspect of the present invention, wherein a polysilicon layer is stacked along thin and thick regions of the gate **insulating** layers.

Brief Description of Drawings Paragraph - DRTX

(7):

[0025] FIG. 6 is an exemplary cross-sectional view showing a step of performing self-aligned trench device isolation at a low voltage part in cell and peripheral regions and a high voltage part of the peripheral region during the formation of a NAND-type flash memory according to an aspect of the present invention, wherein a **photoresist** pattern is removed.

Brief Description of Drawings Paragraph - DRTX

(8):

[0026] FIG. 7 is an exemplary cross-sectional view showing a step of performing self-aligned trench device isolation at a low voltage part in cell and peripheral regions and a high voltage part of the peripheral region during the formation of a NAND-type flash memory according to an aspect of the present invention, wherein the gate **insulating** layers and a silicon substrate are